UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/615,956	07/13/2000	Kumi Miyachi	1248-0509P	3629

7590 02/27/2003

Birch Stewart Kolasch & Birch LLP
P O Box 747
Falls Church, VA 22040-0747

EXAMINER
ABRAHAM, ESAW T

ART UNIT	PAPER NUMBER
2133	8

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/615,956	Applicant(s) MIYACHI ET AL.	
	Examiner Esaw T Abraham	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Final rejection

1. Claims **1 to 14** are presented for examination.

2. The new **title** is acknowledged and entered by the examiner.

Response to the arguments

3. Applicants argument's with respect to amended and added claims 1-14 filled in 11/27/02 have been fully considered but they are not persuasive. Therefore, the rejection in the office action in paper number 5 stands.

Remarks page 10-14, the applicant argues (in claims 1, 2 and 5) that plurality of IC's chips are integrally sealed is unpersuasive in view of Brown et al. figure 2 which chips are integrally sealed in a circuit board. The chips clearly contain IC chips (see figure 2 and col. 13, lines 13-20). In the patent all available slots (where the IC semiconductor devices are located) have direct communication with the test bus and the controller of the system. Therefore, the slot is selected for scan test by a control test signal from the controller and test signal is provided to the selected slot through test input pin. As for claim 5, the obviousness rejection was induced by the absence of similar expression in the patent. The claimed terminologies such as test command data/input terminal may not be exactly presented by the patent. For example, the patent calls the test "command data input" as TDI which is test data input. Other than that there is no literally any difference between both systems. Therefore, the application of the patent in the obviousness rejection is appropriate.

As for claim 3,4 and 7 the applicant clearly discloses plurality of chips in a substrate (board) in slots are directly in contact with the test input signal and of course with the test output

signal. This is because any test input to IC chips must have test output at output end. Therefore, the application of the patent in the obviousness rejection is appropriate. Most of applicant's argument is directed towards the absence of single or multiple chips in contact with said test input signal terminal/s, output signal terminal/s and the test controller through test controller terminal/s. However, the patent clearly teaches the elements in column 12 lines 45-65. In light of the teachings, applicant's arguments have been considered moot. As for the argument Brown teaches only one of the chips being connected to the test input/output and control terminal is also moot in light of the teaching in column 13 lines 10-20 whereby the patent clearly teaches that the slot links (IC chip links) are connected to the test bus in parallel. This means all of the slots; hence, the IC chips in the system are directly in contact with the test bus. The teaching continues such that the slots IC chips (IC chips on board) are selected by the controller, which further asserts that the controller has access to all slots, which also mean there is a connection between each slot and the controller. Brown, however, teaches that only one of the chips is connected to the test signal input. This, however, is another embodiment, which means that a single chip may be selectively tested and does not mean a single chip alone is connected with the test terminal as interpreted by applicant. This arrangement is taught in column 12 lines 44-55 where the test controller "test master" is in a communication with a ring of chips under test. Therefore, the argument has fully considered, but were found unpersuasive.

4. In response to applicant's argument that the examiner has combined an excessive number of references, reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims **1, 2, 8 and 9** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Brown et al (U.S. PN: 5,627,842).

As per claims **1 and 8,** Brown et al. disclose a semiconductor device comprising plurality of chips integrally sealed (see figure 2 and col. 3, lines 49-55), a test signal input terminal for receiving a test signal (see fig. 2, edge connector coupled to the input TDI and col. 4, lines 3-9), a test output terminal for outputting a test result of plurality of chips to outside (see fig. 2, edge connector coupled to the output TDO), a control signal input terminals for receiving a test control signals (see fig. 2, edge connector coupled to the inputs TMS and TCK) whereby the test signal inputted transferred through the plurality of chips (see fig. 2, "input TDI" and col. 4, lines 3-27) and the test control signals inputted being individually supplied to each of said plurality of chips (see fig. 2, "the inputs of TCK and TMS coupled to each of the chips).

As per claims **2 and 9,** Brown et al disclose all subject matter claimed in claim 1 including plurality of chips connected to each other through test output terminal (see col. 4, lines 3-27).

As for using different expressions for the same element it is clear that a pin means a terminal and a terminal in the art is commonly formed by a bump, a contact pad, contact lead, a

contact solder and etc... It is also clear that the slight structure difference between the contact elements is exchangeable in the art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **3-7 and 12-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al (U.S. PN: 5,627,842)

As per claims **3 and 10,** Brown et al. disclose a semiconductor device comprising plurality of chips integrally sealed (see figure 2 and col. 3, lines 49-55), a test signal input terminal for receiving a test signal (see fig. 2, "input TDI" and col. 4, lines 3-9), a test output terminal for outputting a test result of plurality of chips to outside (see fig. 2, "output TDO"), a control signal input terminals for receiving a test control signals (see fig. 2, inputs TMS and TCK), whereby the test signal inputted to one of the plurality of chips and transferred through the other chips (see fig. 2, "input TDI" and col. 4, lines 3-27) and the test control signals inputted being individually supplied to each of the plurality of chips (see fig. 2, the inputs of TCK and TMS coupled to each of the chips).

Brown et al did not explicitly teach a single (only one of the) chip connected to the test signal input terminal and test result output terminal whereby the test signal is transferred to the other chips. However, Brown et al. teach mechanics of testing and capable of transferring data

between on–chip logic side and the pin by which the chip is connected to the rest of the system (other chips) (see col. 4, lines 28-45) which Brown et al's techniques of transferring data is similar to the applicants method. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to use the techniques of transferring test data through a single chip connected to the input/output test terminals. This modification would have been obvious because a person having ordinary skill in the art would have been motivated in order to maximize the system's testing performance.

As for using different expressions for the same element it is clear that a pin means a terminal and a terminal in the art is commonly formed by a bump, a contact pad, contact lead, a contact solder and etc. It is also clear that the slight structure difference between the contact elements is exchangeable in the art.

As per claims **4 and 11,** Brown et al disclose all subject matter claimed in claim 3 including a chip that includes a controller (TAP controller) for controlling an input/output interface of the test signal (see col. Fig. 4, "TAP controller").

As per claims **5 and 12,** Brown et al. disclose a semiconductor device in which a plurality of chips are sealed (see fig. 2) comprising a test registers providing between core logic and the chips (see fig. 2, "the small squares surround the core logics" in each of the chips), a controller (TAP controller) for controlling the test registers and for testing the chip (see col. 4, lines 28-63), a test data input of a device (see fig. 2, edge connector coupled to the input of TDI), a test data output of a device (see fig. 2, edge connector coupled to the output of TDO) and the said test data input connected to the test data input of a first stage (see fig. 2, input of the line TDI) and serially connected to the test data input of a chip of a following stage (see fig. 2, "the

line that connects the four IC's and col. 4, lines 3-27). Brown et al did not explicitly teach a single (only one of the) chip connected to the said test signal input terminal and test result output terminal whereby the test signal is transferred to the other chips. However, Brown et al. teach mechanics of testing and capable of transferring data between on–chip logic side and the pin by which the chip is connected to the rest of the system (other chips) (see col. 4, lines 28-45) which Brown's technique is similar to the applicant's method. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to use the techniques of transferring test data through a single chip connected to the input/output test terminals. This modification would have been obvious because a person having ordinary skill in the art would have been motivated in order to maximize the system's testing performance.

As for using different expressions for the same element it is clear that a pin means a terminal and a terminal in the art is commonly formed by a bump, a contact pad, contact lead, a contact solder and etc. It is also clear that the slight structure difference between the contact elements is exchangeable in the art.

As per claims **6 and 13,** Brown et al disclose a semiconductor device in which plurality of chips sealed (see fig. 2) comprising a test registers providing between core logic and the chips (see fig. 2, "the small squares surrounded the core logic" in each of the chips), a controller (TAP controller) for controlling the test registers and for testing the chip (see col. 4, lines 28-63), a test data input (see fig. 2, edge connector coupled to the input of TDI), a test data output (see fig. 2, edge connector coupled to the output of TDO), a test data input connected to the test data input of a first stage (see fig. 2, input of the line TDI) and serially connected to the test data input of a chip of a following stage (see fig. 2, "the lines that connect the four IC's and col. 4, lines 3-27).

It is unclear whether Brown et al teach a test data device. However, Brown et al teach circuit boards loaded with standard – compliant devices connected together into test rings by local test busses accessible at the edge connectors known entities for down-steam manufacturers and their test engineers (see col. 3, lines 40-42). Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to include a test data device. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to because such test data device in order to test or check responses to both valid and erroneous inputs.

As for using different expressions for the same element it is clear that a pin means a terminal and a terminal in the art is commonly formed by a bump, a contact pad, contact lead, a contact solder and etc... It is also clear that the slight structure differences between the contact elements are exchangeable in the art.

As in claims **7 and 14,** Brown et al. disclose a semiconductor device in which plurality of chips sealed (see fig. 2) comprising a test data input connected to the test data input of a first stage (see fig. 2, input of the line TDI) and serially connected to the test data input of a chip of a following stage (see fig. 2, "the lines that connect the four IC's and col. 4, lines 3-27), a test registers providing between core logic and the chips (see fig. 2, "the small squares surrounded the core logic" in each of the chips), a controller (TAP controller) for controlling the test registers and for testing the chip (see col. 4, lines 28-63), a test data input (see fig. 2, edge connector coupled to the input of TDI) and test data output (see fig. 2, edge connector coupled to the output of TDO). Brown et al did not explicitly teach a single (only one of the) chip connected to the said test signal input terminal and test result output terminal whereby the test signal is

transferred to the other chips. However, Brown et al. teach mechanics of testing and capable of transferring data between on–chip logic side and the pin by which the chip is connected to the rest of the system (including other chips (see col. 4, lines 28-45) which Brown's techniques of transferring data is similar to the applicants method. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to use the techniques of transferring test data through a single chip connected to the input/output test terminals. This modification would have been obvious because a person having ordinary skill in the art would have been motivated in order to maximize the system's testing performance. As for test data relay input/output is common knowledge for most of IC testing systems. Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made use test data relays. This modification would have been obvious because a person having ordinary skill in the art would have been motivated because data relays enable two network systems to use similar functions and different protocols which results in storing and forwarding services rather than a real-time service.

As for using different expressions for the same element it is clear that a pin means a terminal and a terminal in the art is commonly formed by a bump, a contact pad, contact lead, a contact solder and etc. It is also clear that the slight structure difference between the contact elements are exchangeable in the art.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 5,978,945	Muris
US PN: 5,808,877	Jeong et al.
US PN: 6,163,867	Miller et al.
US PN: 6,006,343	Whetsel et al.
US PN: 6,260,165	Whetsel et al.
US PN: 6,199,182	Whetsel et al.
US PN: 5,621,740	Kamada

10. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100